IN THE CLAIMS

Please amend the claims as follows:

Claims 1-143 (Canceled)

144. (New) A semiconductor device comprising:

a first monocrystalline semiconductor layer comprising a first region and a second region;

an electrical semiconductor component positioned at least partially within the first region;

a second monocrystalline compound semiconductor layer overlying the second region; and

a second semiconductor component positioned at least partially within the second monocrystalline compound semiconductor layer.

145. (New) The semiconductor device of claim 144 further comprising a monocrystalline oxide layer positioned between the first region and the second monocrystalline compound semiconductor region.

146. (New) The semiconductor device of claim 145 further comprising an electrical interconnection between the active semiconductor component and the second semiconductor component.

147. (New) The semiconductor device of claim 145 wherein the first monocrystalline semiconductor layer comprises silicon and the monocrystalline oxide layer comprises a material selected from the group consisting of: alkaline earth metal titanates, alkaline earth metal zirconates, and alkaline earth metal hafnates.

148 (New) The semiconductor device of claim 144 further comprising an electrical interconnection between the active semiconductor component and the second semiconductor component.

149. (New) An integrated circuit comprising:

a first accommodating buffer layer;

a first monocrystalline semiconductor layer overlying the first accommodating buffer layer;

a second accommodating buffer layer overlying the first monocrystalline semiconductor layer; and

a second monocrystalline semiconductor layer overlying the second accommodating buffer layer.

150. (New) The integrated circuit of claim 149, wherein:

one of the first and second monocrystalline semiconductor layers is a monocrystalline compound semiconductor layer; and

the other of the first and second monocrystalline semiconductor layers is a monocrystalline Group IV semiconductor layer.

151. (New) The integrated circuit of claim 149, wherein:

the first monocrystalline semiconductor layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the first accommodating buffer layer;

the second accommodating buffer layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the first monocrystalline semiconductor layer; and

the second monocrystalline semiconductor layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the second accommodating buffer layer.

152. (New) The integrated circuit of claim 149, wherein:

the first accommodating buffer layer and the first monocrystalline semiconductor layer have a lattice mismatch no greater than approximately 2.0% and a thickness of the first monocrystalline semiconductor layer is at least approximately 20 nm; and

the second accommodating buffer layer and the second monocrystalline semiconductor layer have a lattice mismatch no greater than approximately 2.0% and a thickness of the second monocrystalline semiconductor layer is at least approximately 20 nm.

153. (New) The integrated circuit of claim 149, further comprising a monocrystalline Group IV substrate underlying the first accommodating buffer layer.

154. (New) An integrated circuit comprising:
an accommodating buffer layer; and
active devices, wherein all the active devices lie at least partially within or over a monocrystalline compound semiconductor layer that overlies the accommodating buffer layer.

155. (New) The integrated circuit of claim 154, wherein:
the integrated circuit includes electronic components;
the electronic components include the active devices active and at least one other component; and
all the electronic components lie at least partially within or over a monocrystalline compound semiconductor layer that overlies the accommodating buffer layer.

156. (New) The integrated circuit of claim 154, wherein the compound semiconductor layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the accommodating buffer layer.

157. (New) The integrated circuit of claim 154, further comprising a monocrystalline Group IV semiconductor substrate that underlies the accommodating buffer layer.

158. (New) The integrated circuit of claim 154, wherein the monocrystalline Group IV semiconductor substrate that is at least approximately 300 millimeters wide.

159. (New) The integrated circuit of claim 154, wherein the accommodating buffer layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the monocrystalline Group IV semiconductor substrate.

160. (New) The integrated circuit of claim 154, wherein the integrated circuit has a feature selected from a group consisting of:

the accommodating buffer layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the monocrystalline Group IV semiconductor substrate; and

the accommodating buffer layer and the monocrystalline Group IV semiconductor substrate have a lattice mismatch no greater than approximately 2.0% and a thickness of the accommodating buffer layer is at least approximately 20 nm.

161. (New) The integrated circuit of claim 154, wherein:

the accommodating buffer layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the monocrystalline Group IV semiconductor substrate; and

the accommodating buffer layer and the monocrystalline Group IV semiconductor substrate have a lattice mismatch no greater than approximately 2.0% and a thickness of the accommodating buffer layer is at least approximately 20 nm.

162. (New) The integrated circuit of claim 154, wherein the accommodating buffer layer and the monocrystalline compound semiconductor layer have a lattice mismatch no greater than approximately 2.0% and a thickness of the monocrystalline compound semiconductor layer is at least approximately 20 nm.